Amendments to the Specification:

Please replace the paragraph beginning on page 1, line 7 with the following amended paragraph:

Error checking of data transmissions between sending and receiving devices use a cyclic redundancy check circuit (CRC) implementing various CRC codes in both the sending and receiving devices. The CRC code is calculated by an exclusive OR (XOR) subtree. As high speed serial interconnect technologies evolve, many of the standards governing these technologies allow bandwidths well beyond the traditional 96 and 128 bits per cycle bandwidths, yet maintain the same transmission frequency as for the older smaller 96 and 128 bits per cycle bandwidths. As bandwidth increases, the complexity and depth of the XOR subtree must increase as the need to process more bits per clock cycle grows. ~~Tradition~~ Traditional CRC designs when applied to large bandwidth data transmissions very quickly develop the interrelated problems of timing closure and physical silicon area required to implement the XOR subtree. Therefore, there is a need for a CRC circuit that can handle large bandwidths without timing closure problems.

Please replace the paragraph beginning on page 2, line 1 with the following amended paragraph:

A first aspect of the present invention is a cyclic redundancy check circuit, comprising: a W-bit packet data slice latch having outputs; a multiple level XOR subtree having inputs and outputs, each level comprising one or more XOR subtrees, each output of the packet data slice latch coupled to an input of the multiple level XOR subtree, each lower level XOR subtree of the multiple level XOR subtree coupled to a higher level XOR subtree of the multiple level XOR subtree through an intervening latch level; a remainder XOR subtree having inputs and outputs; a

combinational XOR subtree having inputs and outputs, the outputs of the remainder XOR subtree and the outputs of the multiple level XOR subtree coupled to the inputs of the combinational XOR subtree; and an M-bit current CRC result latch having inputs and outputs, the output of the combinational XOR subtree coupled to the inputs of the current CRC result latch and the outputs of the M-bit current CRC result latch coupled to the inputs of the remainder XOR subtree.

Please replace the paragraph beginning on page 2, line 13 with the following amended paragraph:

A second aspect of the present invention is a method for cyclic redundancy check calculation, comprising: providing a W-bit packet data slice latch having outputs; providing a multiple level XOR subtree having inputs and outputs, each level comprising one or more XOR subtrees, each output of the packet data slice latch coupled to an input of the multiple level XOR subtree, each lower level XOR subtree of the multiple level XOR subtree coupled to a higher level XOR subtree of the multiple level XOR subtree through an intervening latch level; providing a remainder XOR subtree having inputs and outputs; providing a combinational XOR subtree having inputs and outputs, the outputs of the remainder XOR subtree and the outputs of the multiple level XOR subtree coupled to the inputs of the combinational XOR subtree; and providing an M-bit current CRC result latch having inputs and outputs, the output of the combinational XOR subtree coupled to the inputs of the current CRC result latch and the outputs of the M-bit current CRC result latch coupled to the inputs of the remainder XOR subtree.

Please replace the paragraph beginning on page 9, line 9 with the following amended paragraph:

FIG. 3 is a generic scalable M-bit CRC circuit according to the present invention. In FIG. 3, a CRC circuit **300** includes a [[K-bit]] W-bit packet data slice latch **305**, N^Y M by N-way leaf XOR subtrees **310** and corresponding M-bit latches **315** (N, Y and M are defined *infra*), intermediate levels of M by N-way XOR subtrees and corresponding latches (not shown), N^2 of M by N-way XOR subtrees **320** and corresponding M-bit latches **325**, N M by N-way XOR subtrees **330** and corresponding M-bit latches **335**, a M by N way XOR subtree **340**, an M by 2 way XOR subtree **345**, a remainder XOR subtree **350** and an M-bit current CRC remainder latch **360**. Packet data slice latch **305** is a partition level 0 latch. Latches **315** are partition level 1 latches, latches **315** are partition level (Y-1) latches and latches **335** are partition level Y latches, so there are Y+1 partition levels in CRC circuit **300**. Leaf XOR subtrees **310**, intermediate XOR subtrees (not shown), XOR subtrees **320**, **325** and **340** may be considered to be in a data slice XOR subtree.